

Amendments to the Specification

Please amend the Specification as indicated below.

Please replace the paragraph beginning at the top of page 2 with the following:

~~the~~ The inrush control block K2 ~~could~~ could also monitor the peak value of the input voltage and compare that to the output voltage on Cout and close the relay when the difference is within a predetermined range. When this occurs, inrush current has decayed to normal operating levels and the relay K1 can be closed by a control signal from the UPFC IC with minimal or no surge current through the relay K1. At this point, down stream converters, whether PFC Boost converters or just load DC/DC Converters can be enabled. In the case of the PFC, the control circuit will limit the input current used to charge a bulk capacitor above the input voltage to the regulation point. Although not shown here, many times a second comparator is used to detect that the output voltage is charged to a predetermined minimum level, i.e. the peak AC input at low line; this signal may be logically combined with the inrush control block K2 to control the relay K1 turn-on. However, it is readily apparent that during shutdown, or line dropouts the relay will not open until the output voltage is lower than the input voltage or the absolute value of the output voltage is below a preset minimum. In addition, it is often desired that the circuit detect cycle drops and maintain operation. However, if the applied AC is at high-line, a cycle drop-out could lead to high surge currents, especially if the Boost power supply is still running. The only current limiting functions would be the series resistance of the circuit through the output capacitor Cout. For example, if with a bulk voltage Vbulk of 150VDC, a peak line voltage of 350VAC, and a series resistance of 1 ohm, the surge current could easily reach hundreds of amperes destroying many of the power supply components. It is also readily appreciated that many relays have pull-in/drop-out times measured in milli-seconds. This slow reaction time can cause the same problems as discussed above.

Insert the following two paragraphs preceding the first line of page 6:

Fig. 4C is a schematic diagram, partly in block diagram form of another implementation of the invention shown in Fig. 3;

Fig. 4D is a schematic diagram, partly in block diagram form of yet another implementation of the invention shown in Fig. 3;

At page 6, amend the paragraph that begins at line 17 to read as follows:

Referring now to Figure 3 there is shown a simplified block diagram of a power factor control circuit with inrush current control 85. As shown at 89 in Fig. 3, a power factor corrector circuit 85 is supplied operating power at 89 taken from the input voltage. During startup current is applied to the parallel resistance of passive resistive device 83 in parallel with the active resistive device 82. The active resistive device 82 is not yet turned on due to the delayed on signal from power factor controller 81 through delay 88. Thus, the active resistive device 82 presents a very high resistance in comparison to the passive resistive device 83 such that current flow is substantially through the passive resistive device 83 for the period of delay determined by delay block 88. Note that delay may be a dedicated delay circuit or, alternatively, may be inherent delay caused by circuit component 81. After the predetermined delay, an on signal turns on the power factor corrector 84 and the active resistive device 82; which in turn allows current to flow through the active resistive device 82. The effective resistance of the parallel combination of the passive resistive device 83 and the active resistive device is determined by the effective resistance of the active resistive device 82 in the on state in parallel with passive resistive device. Advantageously, the resistance of the active resistive device 82 in the on state is very low with respect to the resistance of the passive device 83.

At page 7, line 30, insert the following new paragraph:

The gate driver for the IGBT can include a power amplifier (Fig. 4C) or a floating power supply (Fig. 4D). Each is known in the art.

Amendments to the Drawings

Please add the accompanying two new drawing sheets bearing new Figs. 4C and 4D to the drawings presently in this application.

Please replace sheet 3/8 bearing Fig. 3 with the accompanying new sheet 3/10 bearing revised Fig. 3. The revision to Fig. 3 adds the reference numeral 89. This conforms Fig. 3 to the amendment to the specification at page 6.

Please replace sheets 1/8, 2/8 and 4/8 - 8/8 with the replacement sheets numbered 1/10, 2/10 and 4/10 - 8/10, the replacement sheets numbering being changed as appropriate with the addition of the two new sheets of drawings.